I, the undersigned, who have prepared English translation which is attached herewith, hereby declare that the aforementioned translation is true and correct translation of officially certified copy of the Korean Patent Application No. 2001-72687 filed on November 21, 2001.

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[Abstract of the Disclosure]

[Abstract]

A MOS transistor having a T-shaped gate electrode includes a gate electrode disposed in the shape of T on a semiconductor substrate; an L-shaped lower spacer disposed at both sides of the gate electrode to cover a top surface of the semiconductor substrate; and low-, mid-, and high-concentration impurity regions formed in the semiconductor substrate of both sides of the gate electrode. The high-concentration impurity region is disposed in the semiconductor substrate next to the lower spacer and the mid-concentration impurity region is disposed between the high- and low-concentration impurity regions. The method of fabricating the MOS transistor includes forming a gate electrode in the shape of T on a semiconductor substrate, then forming a low-concentration impurity region in the semiconductor substrate of both sides of the gate electrode. An L-shaped lower spacer is disposed at both sides of the gate electrode to have a horizontal projection extended over the low-concentration impurity region. By using the L-shaped lower spacer and a gate pattern as an ion implantation mask, high- and mid- concentration impurity regions are formed.

[Typical Figure]

FIG. 9

[Specification]

[Title of the Invention]

MOS TRANSISTOR WITH T-SHAPED GATE ELECTRODE AND METHOD OF FABRICATING THE SAME

[Brief Description of the Drawings]

Figs. 1 and 2 are cross-sectional views for explaining MOS transistors in accordance to prior arts.

Figs. 3 through 8 are cross-sectional views for explaining a method of fabricating a MOS transistor having a T-shaped gate electrode in accordance to a preferred embodiment of the present invention; and

Fig. 9 is a perspective view showing the MOS transistor having the T-shaped gate electrode in accordance to the preferred embodiment of the present invention.

[Detailed Description of the Invention]

[Object of the Invention]

[Field of the Invention and Prior Art related to the Invention]

The present invention relates to a semiconductor device and a method of fabricating the same and, more particularly, to a MOS transistor having a T-shaped gate electrode and a method of fabricating the same.

Semiconductor devices are becoming increasingly in need of high integration and high-speed characteristics with developments in electronic industries. To meet such requirements, MOS transistors with various structures have been used for the semiconductor devices. However, the semiconductor devices with conventional MOS transistors cannot completely fulfill the high integration and high-speed characteristics.

Fig. 1 is a cross-sectional view of a conventional MOS transistor.

Referring to Fig. 1, a gate oxide layer 12 and a gate pattern 14 are sequentially stacked on a semiconductor substrate 10. A gate spacer 16 is disposed on both sidewalls of the gate pattern 14. A high-concentration impurity region 20 is disposed in the semiconductor substrate next to the gate spacer 16.

As the gate pattern 14 has become gradually finer with the high integration of the semiconductor device, an interval between the high-concentration impurity regions 20, i.e., an interval between source and drain regions has been gradually reduced. This results in a short channel effect that seriously causes degradation of characteristics of the semiconductor devices.

Generally, to minimize such a short channel effect, a low-

concentration impurity region 18 has been formed in the semiconductor substrate 10 under the gate spacer 16 as shown in Fig. 1. The structure having the high- and low- concentration impurity regions 20 and 18 is normally called "lightly doped drain (LDD) structure".

However, even if the LDD structure may minimize the short channel effect caused by shrinking a width of the gate pattern 14, it is still difficult to shrink the width of the gate pattern 14 due to technical limitations. In addition, the fineness of the gate pattern 14 may cause other problems than the short channel effect, i.e., may increase not only a resistance of a gate line, but also a capacitance between the gate pattern 14 and the high-concentration impurity region 20. Consequently, as the gate pattern 14 becomes gradually finer, it becomes more difficult to fabricate the semiconductor device of high speed.

Fig. 2 is a cross-sectional view of a MOS transistor with T-shaped gate electrode, which has been recently proposed. An example of the MOS transistor with the T-shaped gate electrode is disclosed by T. Ghani et al. in "100nm gate length high performance/low power CMOS transistor structure", IEDM Technical Digest, 1999, pp. 415-418.

Referring to Fig. 2, a gate oxide layer 32 and a gate pattern 34 are sequentially stacked on a semiconductor substrate 30. The gate pattern 34 is a T-shaped structure including an undercut region. A gate spacer 36 is disposed on both sidewalls of the gate pattern 34 to fill the undercut region. A high-concentration impurity region 40 is disposed in the semiconductor

substrate 30 next to the gate spacer 36. A low-concentration impurity region 38 is disposed in the semiconductor substrate 30 under the gate spacer 36 and the undercut region.

In the MOS transistor having the gate pattern 34 as shown in Fig. 2, an interval between the high-concentration impurity region 40 and the gate pattern 34 is wider as much as about a width of the undercut region as compared with the MOS transistor of Fig. 1. Accordingly, a capacitance between the gate pattern 34 and the high-concentration impurity region 40 may be reduced. In addition, a channel width of the semiconductor device may be reduced as much as the width of the undercut region.

Unfortunately, however, a width of the low-concentration impurity region 38 is increased as much as the width of the undercut region. This results in a problem like an increase in a source/drain resistance R_{sd} of the transistor.

[Technical Object of the Invention]

It is therefore a feature of the present invention to provide a method of fabricating a MOS transistor having a T-shaped gate electrode that can minimize a source/drain resistance.

It is another feature of the present invention to provide a MOS transistor including a mid-concentration impurity region that can minimize a source/drain resistance.

[Construction of the Invention]

The present invention provides a method of fabricating the MOS transistor comprising forming the mid-concentration impurity region by use of an L-shaped spacer. The method comprises forming the T-shaped gate electrode on a semiconductor substrate, then forming a low-concentration impurity region in the semiconductor substrate of both sides of the gate electrode. An L-shaped lower spacer is disposed at both sides of the gate electrode to have a horizontal projection extended over the low-concentration impurity region. By using the L-shaped lower spacer and a gate pattern as an ion implantation mask, high- and mid- concentration impurity regions are formed.

Preferably, forming the T-shaped gate electrode comprises forming lower and upper conductive layer patterns that are sequentially stacked, then selectively etching the lower conductive layer pattern. It is therefore preferable that the lower and upper conductive layer patterns are made of materials having an etch selectivity with respect to each other. For example, the lower conductive layer pattern is preferably made of silicon germanium or nitride titanium and the upper conductive layer pattern is made of polysilicon or tungsten. It is also preferable that the selective etching of the lower conductive layer pattern employs an isotropic etch process. Thus, an undercut region is formed under an edge of the upper conductive layer pattern.

Forming the L-shaped lower spacer comprises sequentially

conformally forming lower, intermediate, and upper insulating layers on an entire surface of the semiconductor substrate having the T-shaped gate electrode. The lower, intermediate, and upper insulating layers are successively etched to form L-shaped lower and intermediate spacers and an upper spacer. Thereafter, the upper and intermediate spacers are removed. In this case, the upper spacer is preferably formed by etching the upper insulating layer using an anisotropic etch process.

The lower spacer is preferably made of one selected from the group consisting of nitride, oxide nitride, and polysilicon. The intermediate and upper spacers are preferably made of materials having etch selectivities with respect to the lower and intermediate spacers, respectively.

The present invention also provides a MOS transistor with a T-shaped gate electrode that includes an L-shaped spacer as well as a mid-concentration impurity region. The MOS transistor includes the T-shaped gate electrode; an L-shaped lower spacer; and low-, mid-, and high-concentration impurity regions. The T-shaped gate electrode is disposed on the semiconductor substrate. The L-shaped lower spacer is disposed at both sides of the gate electrode to cover the top surface of the semiconductor substrate. The low-, mid-, and high- concentration impurity regions are formed in the semiconductor substrate of both sides of the gate electrode. The high-concentration impurity region is disposed in the semiconductor substrate next to the lower spacer, and the mid-concentration impurity region is intervened between the high- and low- concentration impurity regions.

The gate electrode may be formed of lower and upper conductive layer patterns that are sequentially stacked. The upper conductive layer pattern is preferably wider than the lower conductive layer pattern so as to have an undercut region at a lower portion thereof. The lower spacer may further have a horizontal extension filling the undercut region.

The lower and upper conductive layer patterns are preferably made of materials having an etch selectivity with respect to each other. For instance, the lower conductive layer pattern is made of silicon germanium or nitride titanium and the upper conductive layer pattern is made of polysilicon or tungsten.

A surface insulating layer may be intervened between the gate electrode and the lower spacer.

The present invention will now be described more fully hereinafter with reference to the accompanying drawings, in which preferred embodiments of the invention are shown. The invention may, however, be embodied in different forms and should not be construed as limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art. In the drawings, the thickness of layers and regions are exaggerated for clarity. It will also be understood that when a layer is referred to as being "on" another layer or substrate, it can be directly on the other layer or substrate, or intervening layers may also be present. Like numbers refer to like elements throughout.

Figs. 3 through 8 are cross-sectional views for explaining the method of fabricating the MOS transistor in accordance to the preferred embodiment of the present invention.

Referring to Fig. 3, a device isolation layer pattern (not shown) is formed at a predetermined region of a semiconductor substrate 100 to define an active region. A gate oxide layer 110 is formed on the active region. A gate conductive layer is formed on an entire surface of the semiconductor substrate having the gate oxide layer 110. The gate conductive layer is then patterned until the gate oxide layer 110 is exposed such that a gate pattern 140 is formed across the active region. At this time, the gate pattern 140 is formed in the shape of T to have an undercut region.

It is preferable that the gate oxide layer 110 is formed by thermally oxidizing the exposed active region of the semiconductor substrate 100. The gate conductive layer is preferably formed of lower and upper conductive layers that are sequentially stacked on an entire surface of the semiconductor substrate having the gate oxide layer 110. To form the gate pattern 140 having the undercut region, the upper and lower conductive layers are patterned to form lower and upper conductive layer patterns 120 and 130 that are sequentially stacked, then selectively etching the lower conductive layer pattern 120. In this case, the selective etching for forming the undercut region preferably employs an isotropic etch process. In addition, another method for forming the undercut region comprises forming the upper conductive layer pattern 130, then etching the lower conductive layer using

the isotropic etch process. As a result, the undercut region where sides of the lower conductive layer pattern 120 are etched is formed under the upper conductive layer pattern 130. The upper and lower conductive layer patterns 130 and 120 constitute the gate pattern 140.

In the etching step for forming the gate pattern 140, the lower conductive layer pattern 120 and the gate oxide layer 110 are preferably made of materials having an etch selectivity with respect to each other in order to minimize etching damages of the semiconductor substrate 100. Likewise, in the selective etching for forming the undercut region, the lower conductive layer pattern 120 is preferably made of a material having etch selectivities with respect to the upper conductive layer pattern 130 and the gate oxide layer 110 to prevent the etching damages.

Considering the etch selectivities between the material layers 110, 120, and 130, the lower and upper conductive layer patterns 120 and 130 are preferably made of silicon germanium and polysilicon, respectively. Alternatively, the lower and upper conductive layer patterns 120 and 130 are preferably made of nitride titanium and tungsten, respectively.

Meanwhile, the gate pattern 140 may be a single layer made of one material other than the foregoing double layer of lower and upper conductive layer patterns 120 and 130. In this case, the gate pattern 140 is preferably a material layer having both conductivity and an etch selectivity with respect to the gate oxide layer 110. Therefore, the gate pattern 140 is preferably

made of polysilicon.

To form the undercut region, the gate pattern 140 may be formed using a dry etching process having an etch selectivity with respect to the gate oxide layer 110. At this time, an etch gas of a plasma phase used for the dry etching process is irregularly reflected from the gate oxide layer 110 such that the undercut region is formed at the gate pattern 140.

Referring to Fig. 4, a semiconductor substrate having the gate pattern 140 is thermally oxidized to cure the damages that occur during the etching for forming the gate pattern 140. Thus, a surface insulating layer 150 is conformally formed on an exposed surface of the gate pattern 140 where the undercut region is formed. The surface insulating layer 150 may be formed also on the exposed gate oxide layer 110 of both sides of the gate pattern 140.

By using the gate pattern 140 as an ion implantation mask, low-concentration impurity ions are implanted into the semiconductor substrate having the surface insulating layer 150. Thus, a low-concentration impurity region 160 is formed in the semiconductor substrate 100 of both sides of the gate pattern.

It is preferable that the low-concentration impurity region 160 is formed also under the undercut region. For this, the low-concentration impurity ions may be implanted into the semiconductor substrate 100 using an oblique ion implantation. In the low-concentration ion implantation process, the gate oxide layer 110 and the surface insulating layer 150 are

used to prevent ion channeling.

Referring to Fig. 5, a lower insulating layer 170, an intermediate insulating layer 180, and an upper insulating layer 190 that are sequentially stacked are conformally formed on an entire surface of the semiconductor substrate having the low-concentration impurity region 160.

Thus, the lower insulating layer 170 covers an entire surface of the surface insulating layer 150 and also fills the undercut region of the gate pattern 140. In case the undercut region is narrow, the surface insulating layer 150 alone may fill the undercut region.

At this time, the lower insulating layer 170 is preferably a material layer having an etch selectivity with respect to an oxide layer such as the gate oxide layer 110, the surface insulating layer 150, and the like. In addition, the intermediate insulating layer 180 is preferably a material layer having an etch selectivity with respect to the lower insulating layer 170, and the upper insulating layer 190 is preferably a material layer having an etch selectivity with respect to the intermediate insulating layer 180. Preferably, the lower insulating layer 170 is made of one selected from the group consisting of nitride, oxide nitride, and polysilicon. The intermediate insulating layer 180 and the upper insulating layer 190 are preferably an oxide layer and a nitride layer, respectively.

The intermediate insulating layer 180 is used to protect the lower insulating layer 170 during a subsequent step for removing the upper

insulating layer 190. Therefore, in the event that the upper insulating layer 190 and the lower insulating layer 170 have an etch selectivity with respect to each other, the intermediate insulating layer 180 may not be formed.

Referring to Fig. 6, the upper, intermediate, and lower insulating layers 190, 180, and 170 are successively etched using an anisotropic etch process until the surface insulating layer 150 is exposed. Thus, the upper insulating layer 190 forms an upper spacer 195 of a normal shape. By contrast, the intermediate and lower insulating layers 180 and 170 form L-shaped intermediate and lower spacers 185 and 175, respectively.

In this case, the L-shaped lower and intermediate spacers 175 and 185 have horizontal projections disposed under the upper spacer 195. That is, the intermediate spacer 185 is disposed on the horizontal projection of the lower spacer 175, and the upper spacer 195 is disposed on the horizontal projection of the intermediate spacer 185.

In the foregoing etching, the intermediate and lower spacers 185 and 175 may be formed using the isotropic etch process. Though, the etching for forming the upper spacer 195 still employs the anisotropic etch process.

Referring to Fig. 7, the upper spacer 195 is removed using an etch recipe having etch selectivities with respect to the intermediate spacer 185 and the surface insulating layer 150. The intermediate spacer 185 is then removed using an etch recipe having etch selectivities with respect to the lower spacer 175 and the gate pattern 140.

The upper and intermediate spacers 195 and 185 are preferably removed using the isotropic etch processes. In case the intermediate spacer 185 is an oxide layer, the surface insulating layer 150 and the gate oxide layer 110, which are also oxide layers, may be etched together while the intermediate spacer 185 is removed. Accordingly, in the foregoing isotropic etch process, a surface insulating layer pattern 155 and a gate oxide layer pattern 115 are etched to form an undercut region under the lower spacer 175 as shown in Fig. 7. As a result, both a top surface of the gate pattern 140 and the semiconductor substrate 100 next to the lower spacer 175 are exposed. For the same reason, a top surface of the surface insulating layer pattern 155 is lower than the gate pattern 140.

By using the gate pattern 140 and the lower spacer 175 as an ion implantation mask, high-concentration impurity ions are implanted into the resultant structure where the intermediate spacer 185 is removed. Thus, a high-concentration impurity region 200 is formed in the semiconductor substrate 100 next to the lower spacer 175. At this time, the horizontal projection of the lower spacer 175 is used to reduce energies of the implanted ions during the high-concentration ion implantation. As a result, a mid-concentration impurity region 205 is formed under the horizontal projection of the lower spacer 175. The mid-concentration impurity region 205 has lower concentration than the high-concentration impurity region 200.

Impurity concentration of the mid-concentration impurity region 205 is dependent upon a thickness of the horizontal projection of the lower

spacer 175, i.e., a thickness of the lower insulating layer 170. Accordingly, a thickness of the lower insulating layer 170 is determined in consideration of the concentration of the mid-concentration impurity region 205.

In addition, an interval between the high-concentration impurity region 200 and the gate pattern 140 is dependent upon a length of the horizontal projection of the lower spacer 175. The length of the horizontal projection of the lower spacer 175 is dependent upon thicknesses of the intermediate and upper insulating layers 180 and 190.

However, in the event that the upper and lower spacers 195 and 175 are made of the same material, a sidewall of the horizontal projection of the lower spacer 175 is etched together while the upper spacer 195 is removed using the isotropic etch process. Therefore, thicknesses of the intermediate and upper insulating layers 180 and 190 are preferably determined in consideration of a length of the recessed horizontal projection of the lower spacer 175.

Referring to Fig. 8, a junction region silicide 210 and a gate silicide 215 are formed on the exposed high-concentration impurity region 200 and the gate pattern 140, respectively, according to a conventional method.

The junction region silicide 210 and the gate silicide 215 are preferably made of one selected from the group consisting of cobalt silicide, nickel silicide, and tungsten silicide. As mentioned above, since the top surface of the surface insulating layer pattern 155 is lower than the gate

pattern 140, the gate pattern 140 is more exposed during the silicidation process. Thus, more atoms of silicon react during the silicidation process. As a result, the gate silicide 215 can be stably formed without being cut due to fineness of the gate pattern 140.

Fig. 9 is a perspective view for explaining the MOS transistor in accordance to the preferred embodiment of the present invention.

Referring to Fig. 9, a device isolation layer pattern 500 is disposed at a predetermined region of the semiconductor substrate 100 to define an active region. A gate oxide layer pattern 115 is disposed on a predetermined portion of the active region.

A T-shaped gate pattern 140 having the undercut region is disposed on the gate oxide layer pattern 115 across the device isolation layer pattern 500. A gate silicide 215 may be further disposed on the gate pattern 140.

A lower spacer 175 is disposed at both sides of the gate pattern 140 to have a horizontal projection extended over the gate oxide layer pattern 115. A surface insulating layer pattern 155 is intervened between the lower spacer 175 and the gate pattern 140 and also between the lower spacer 175 and the gate oxide layer pattern 115. In particular, the surface insulating layer pattern 155 fills the undercut region of the gate pattern 140 together with the lower spacer 175. For this, the lower spacer 175 may further have a horizontal extension extended to the undercut region.

A high-concentration impurity region 200 separated from the gate

pattern 140 is disposed in a semiconductor substrate 100 next to the lower spacer 175. A junction region silicide 210 may be further disposed on the high-concentration impurity region 200.

A low-concentration impurity region 160 is disposed in the semiconductor substrate 100 under the undercut region of the gate pattern 140. Also, a mid-concentration impurity region 205 is disposed in the semiconductor substrate 100 under the horizontal projection of the lower spacer 175. That is, the mid-concentration impurity region 205 is intervened between the high- and low- concentration impurity regions 200 and 160.

[Effect of the Invention]

According to the present invention, using the L-shaped spacer formed at both sides of the T-shaped gate electrode, the mid-concentration impurity region is formed between the high- and low- concentration impurity regions. As a result, it is possible to obtain advantages of the transistor with the T-shaped gate electrode, i.e., a decrease in a capacitance, a decrease in a channel length, and an increase in a cross-sectional area of the gate electrode. At the same time, it is also possible to obtain an advantage of the mid-concentration impurity region, i.e., a decrease in a source/drain resistance R_{sd}.

[Scope of the Claim]

[Claim 1]

A method of fabricating an MOS transistor, comprising:

forming a T-shaped gate electrode on a semiconductor substrate;

implementing a low-concentration ion implantation process using the gate electrode as an ion implantation mask to form a low-concentration impurity region in the semiconductor substrate of both sides of the gate electrode;

sequentially forming an L-shaped lower spacer, an L-shaped intermediate spacer, and an upper spacer on the low-concentration impurity region of the both sides of the gate electrode;

removing the upper and intermediate spacers to expose the lower spacer; and

implementing a high-concentration ion implantation process into the semiconductor substrate where the lower spacer is exposed to form high- and mid- concentration impurity regions.

[Claim 2]

The method as claimed in Claim 1, wherein forming the T-shaped gate electrode comprises:

forming lower and upper conductive layer patterns that are sequentially stacked on the semiconductor substrate; and

selectively etching the lower conductive layer pattern such that an undercut region is formed under an edge of the upper conductive layer pattern.

[Claim 3]

The method as claimed in Claim 2, wherein the lower and upper conductive layer pattern are made of materials having an etch selectivity with respect to each other.

[Claim 4]

The method as claimed in Claim 2, wherein the lower conductive layer pattern is made of silicon germanium or nitride titanium.

[Claim 5]

The method as claimed in Claim 2, wherein the upper conductive layer pattern is made of polysilicon or tungsten.

[Claim 6]

The method as claimed in Claim 2, wherein the selective etching of

the lower conductive layer pattern employs an isotropic etch process.

[Claim 7]

The method as claimed in Claim 1, further comprising conformally forming a surface insulating layer on an entire surface of the semiconductor substrate having the gate electrode.

[Claim 8]

The method as claimed in Claim 1, wherein the lower spacer is made of one selected from the group consisting of nitride, oxide nitride, and polysilicon.

[Claim 9]

The method as claimed in Claim 1, wherein the intermediate spacer is made of a material having an etch selectivity with respect to the lower spacer.

[Claim 10]

The method as claimed in Claim 1, wherein the upper spacer is made of a material having an etch selectivity with respect to the intermediate

spacer.

[Claim 11]

The method as claimed in Claim 1, wherein forming the upper, intermediate, and lower spacers comprises:

conformally forming lower, intermediate, and upper insulating layers that are sequentially stacked on an entire surface of the semiconductor substrate having the T-shaped gate electrode; and

successively etching the upper, intermediate, and lower insulating layers, wherein the upper insulating layer is etched using an anisotropic etch process.

[Claim 12]

The method as claimed in Claim 1, further comprising forming a gate oxide layer on an entire surface of the semiconductor substrate before forming the gate electrode.

[Claim 13]

The method as claimed in Claim 1, implementing the high-concentration ion implantation process is followed by forming a junction

region silicide and a gate silicide at the high-concentration impurity region and on the upper conductive layer pattern, respectively.

[Claim 14]

A MOS transistor comprising:

a T-shaped gate electrode disposed on a semiconductor substrate;

an L-shaped lower spacer covering a top surface of the semiconductor substrate at both sides of the gate electrode;

a low-concentration impurity region formed in the semiconductor substrate of both sides of the gate electrode;

a high-concentration impurity region formed in the semiconductor substrate next to the lower spacer; and

a mid-concentration impurity region disposed between the high- and low- concentration impurity regions.

[Claim 15]

The MOS transistor as claimed in Claim 14, wherein the gate electrode comprises lower and upper conductive layer patterns that are sequentially stacked, wherein the upper conductive layer pattern is wider than the lower conductive layer pattern so as to have an undercut region at a

lower portion of the upper conductive layer pattern.

[Claim 16]

The MOS transistor as claimed in Claim 15, wherein the lower spacer further comprises a horizontal extension filling the undercut region.

[Claim 17]

The MOS transistor as claimed in Claim 15, wherein the lower and upper conductive layer patterns are made of materials having an etch selectivity with respect to each other.

[Claim 18]

The MOS transistor as claimed in Claim 15, wherein the lower conductive layer pattern is made of silicon germanium or nitride titanium.

[Claim 19]

The MOS transistor as claimed in Claim 15, wherein the upper conductive layer pattern is made of polysilicon or tungsten.

[Claim 20]

The MOS transistor as claimed in Claim 14, further comprising a surface insulating layer intervened between the gate electrode and the lower spacer.

Fig. 1

(Prior Art)

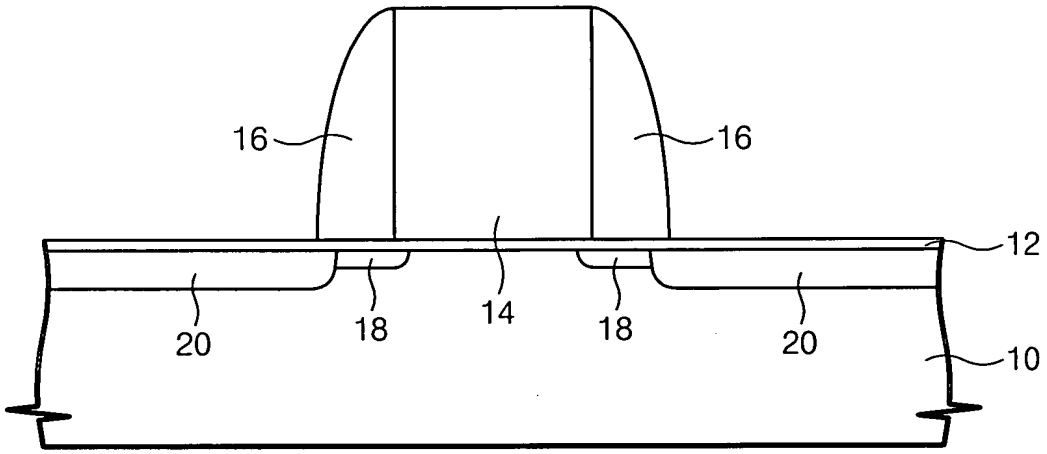

Fig. 2

(Prior Art)

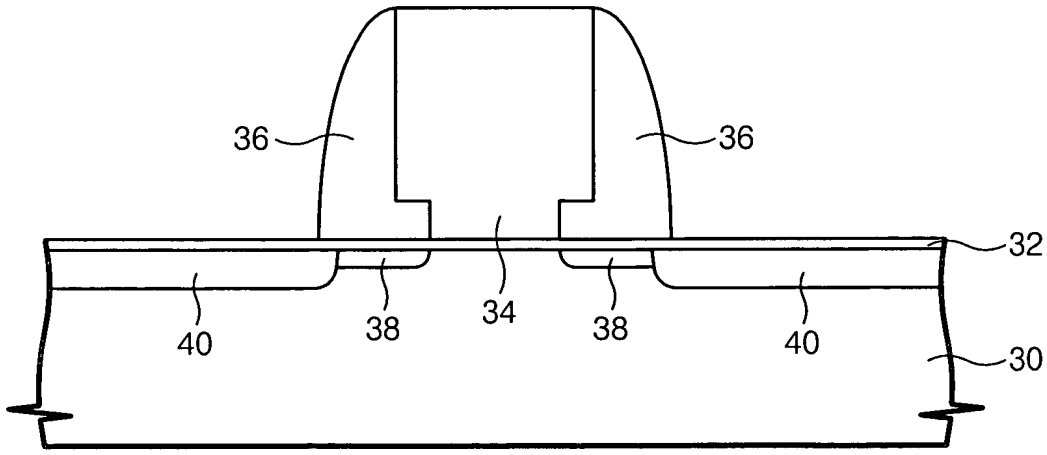

Fig. 3

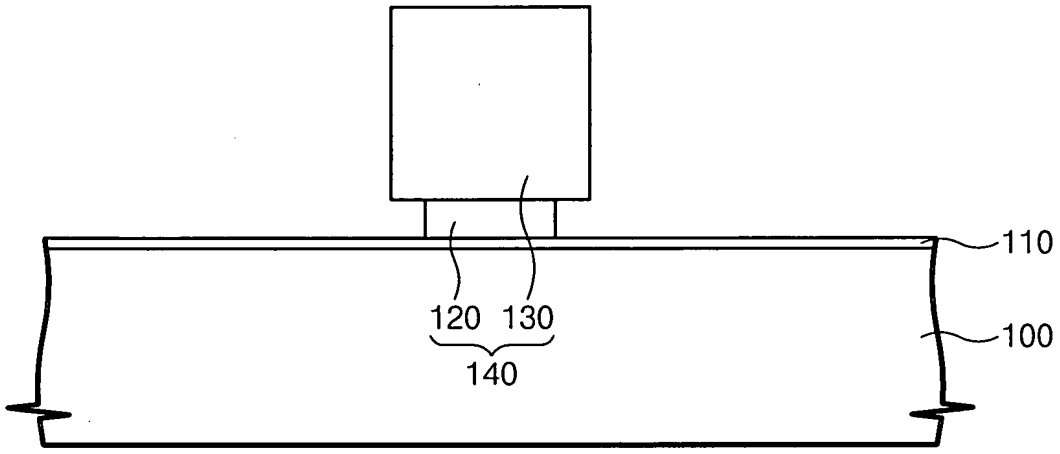

Fig. 4

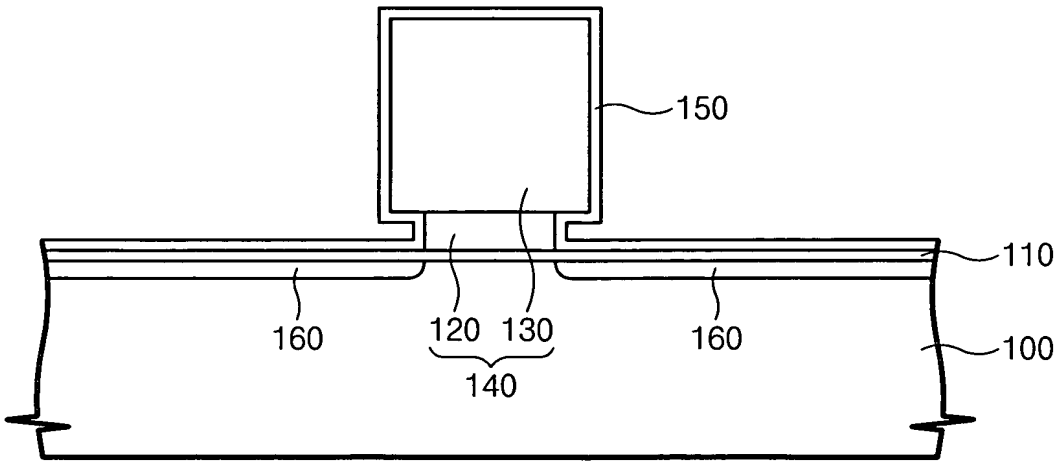

Fig. 5

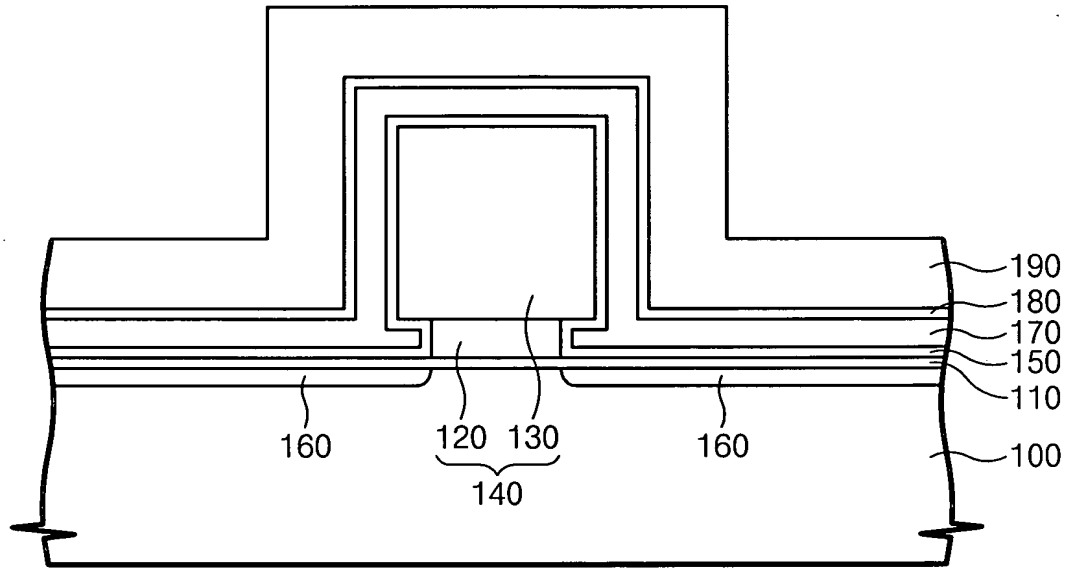
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Fig. 6

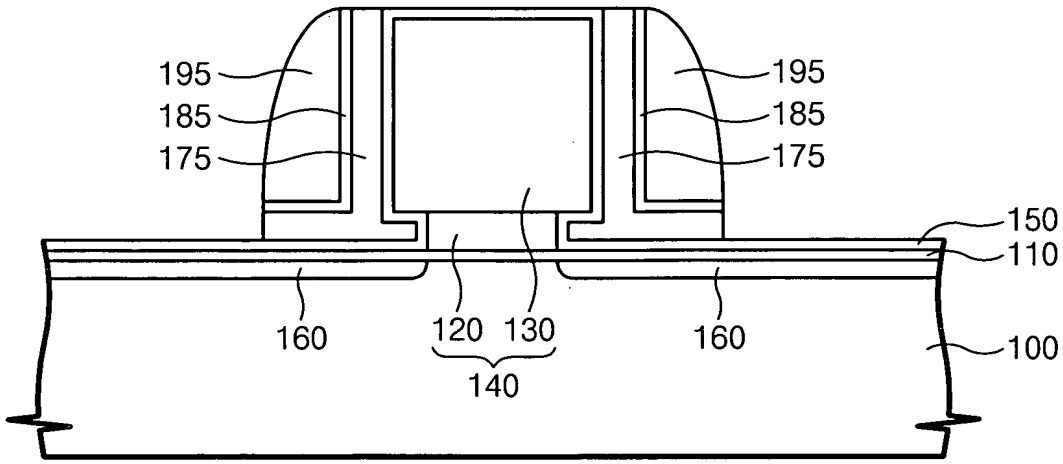
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Fig. 7

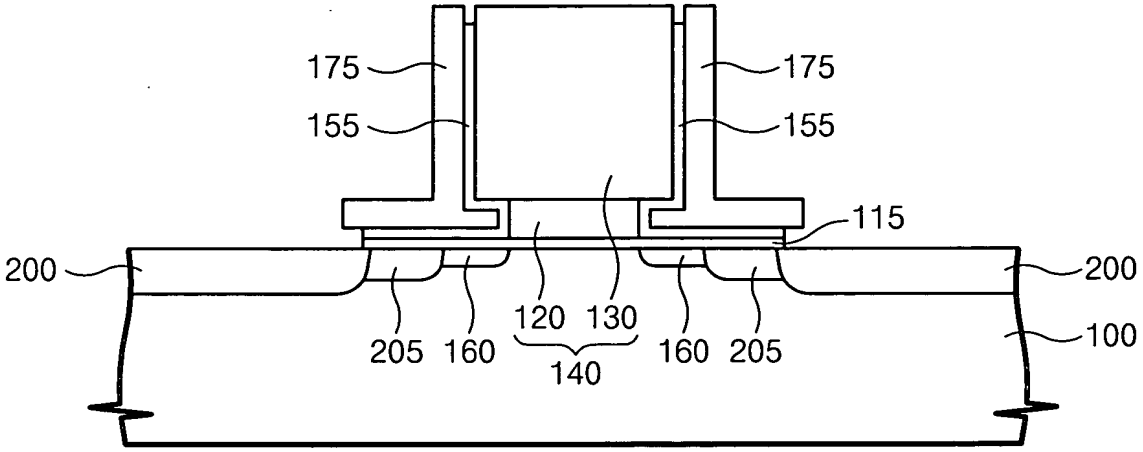
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Fig. 8

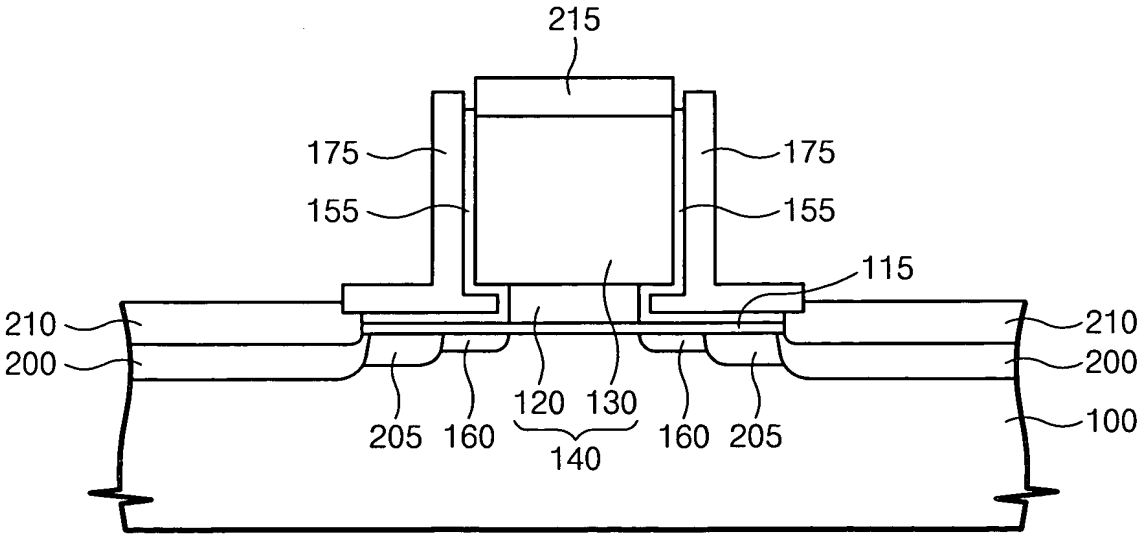
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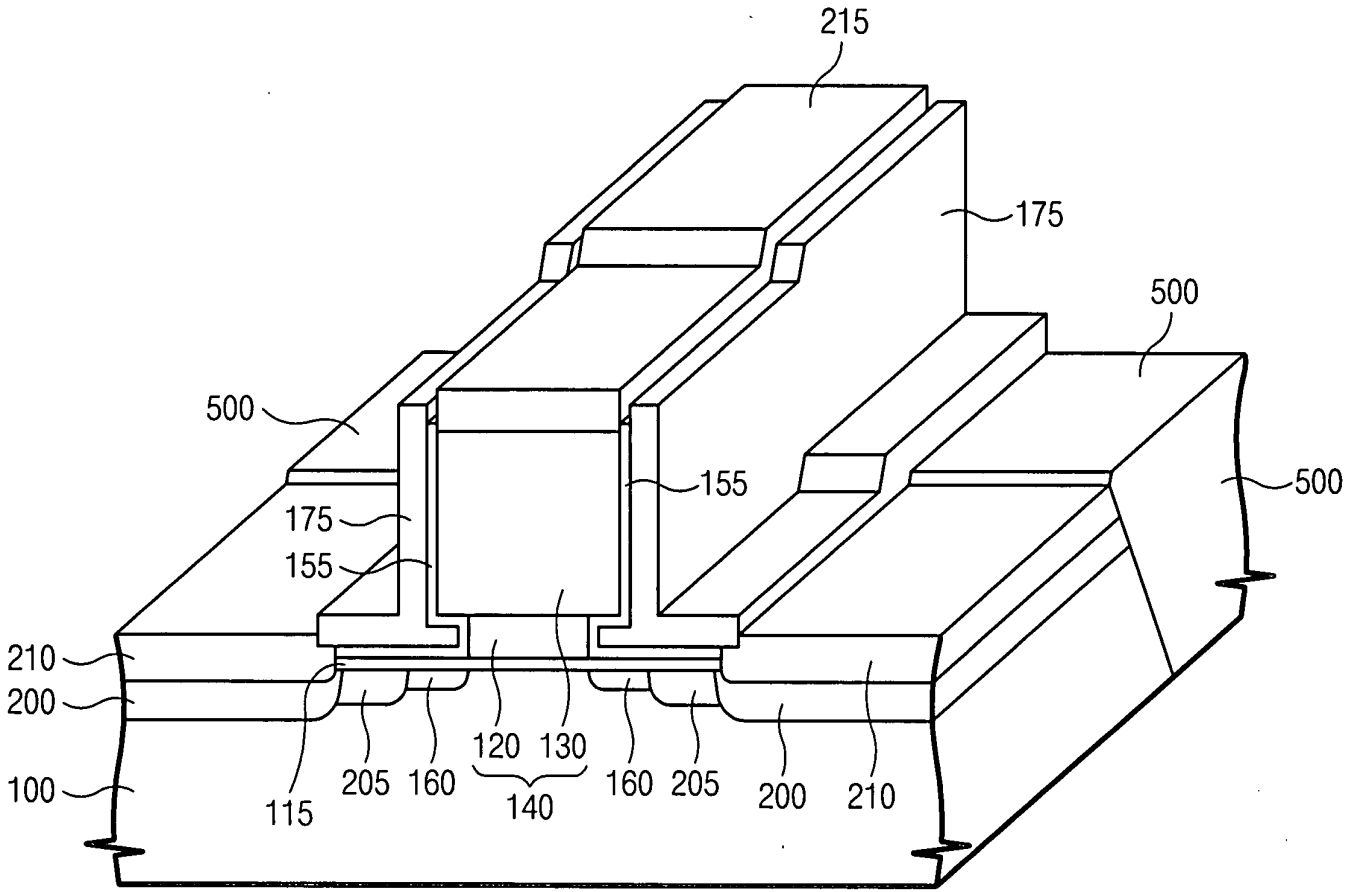
Fig. 9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